Lab 3: Combinational Design

**Primary Objectives:**

1. Get experience simplifying Boolean equations.
2. Implement and test a simplified circuit that outputs the largest 2-bit value given 2 2-bit inputs. (2-bit priority selector)

**Design**

Table 1: Symbol Mapping

|  |  |
| --- | --- |
| Name | Symbol |
| A | A |
| B | B |
| Least Significant Bit of A | A0 |
| Most Significant Bit of A | A1 |
| Least Significant Bit of B | B0 |
| Most Significant Bit of B | B1 |
| C | C |
| Least Significant Bit of C | C0 |
| Most Significant Bit of C | C1 |

Table 1 lists the symbols used in the rest of the document

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A1 | A0 | B1 | B0 | C1 | C0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Table 2: Truth table for the 2-bit priority selector

Table 2 describes all possible outcomes for this device, the table specifically shows that C will always output the greater of A and B.

Boolean Expression of the truth table

C1 = A1’A0’B1B0’ + A1’A0’B1B0 + A1’A0B1B0’ + A1’A0B1B0 + A1A0’B1’B0’ + A1A0’B1’B0 + A1A0’B1B0’ + A1A0’B1B0 + A1A0B1’B0’ + A1A0B1’B0 + A1A0B1B0’ + A1A0B1B0

C0 = A1’A0’B1'B0 + A1’A0’B1B0 + A1’A0B1’B0’ + A1’A0B1’B0 + A1’A0B1B0 + A1A0’B1B0 + A1A0B1’B0’ + A1A0B1’B0 + A1A0B1B0’ + A1A0B1B0

Simplifying the Boolean Expressions with K-maps

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| C1 | B1B0 | | | | |
| A1A0 |  | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 1 | 1 |
| 01 | 0 | 0 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

C1 = A1 + B1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| C0 | B1B0 | | | | |
| A1A0 |  | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 0 |
| 01 | 1 | 1 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 0 |

C0 = A1’B0 + A0B1’ + A1A0 + B1B0

**Implementation**

Figure 1: Implemented 2-bit priority selector

Diagram

Description automatically generated

The 2-bit priority selector is implemented as seen above in figure 1 with each output labeled.

**Testing**

Table 3: Log of outputs from the designed device

|  |  |  |
| --- | --- | --- |
| A | B | C |
| 00 | 00 | 00 |
| 01 | 00 | 01 |
| 11 | 00 | 11 |
| 10 | 00 | 10 |
| 10 | 01 | 10 |
| 11 | 01 | 11 |
| 01 | 01 | 01 |
| 00 | 01 | 01 |
| 00 | 11 | 11 |
| 01 | 11 | 11 |
| 11 | 11 | 11 |
| 10 | 11 | 11 |
| 10 | 10 | 10 |
| 11 | 10 | 11 |
| 01 | 10 | 10 |
| 00 | 10 | 10 |

The log is similar to the truth table seen above in table 2. This demonstrates that the implemented design functions appropriately.

**Conclusion**

Experience simplifying Boolean expressions has been gained, and the device works as expected. The circuit outputs the largest 2-bit value given 2 2-bit inputs.